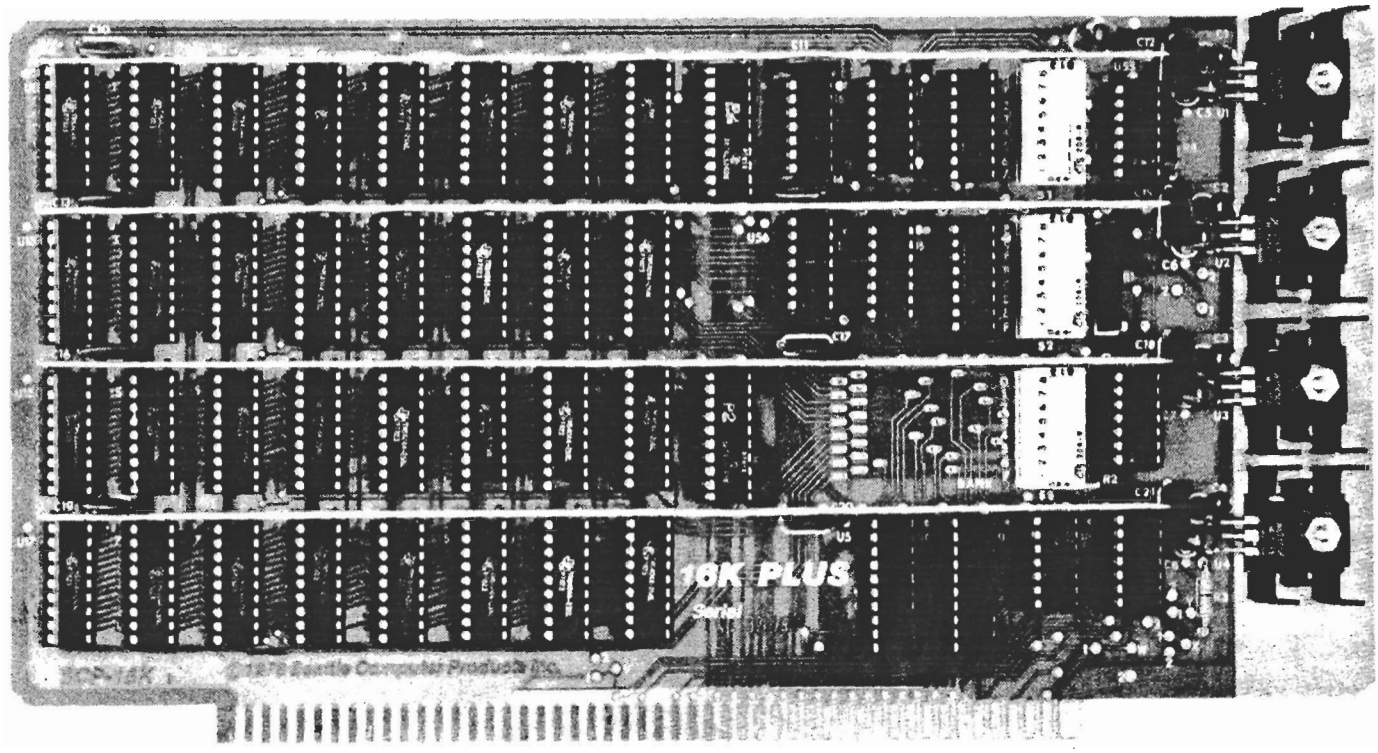
Instruction Manual



16K PLUS

High Reliability 16K RAM

The 16K PLUS 16K by 8 bit fully static RAM board was designed to provide a highly reliable memory with maximum compatibility with the S-100 bus. It was designed to be easy to use, easy to repair in the event of a malfunction, and to have a high benefit to cost ratio.

It incorporates state-of-the-art features such as Schmitt trigger buffers for all signal inputs, DIP switch addressing with the capability of being "parallel addressed", and it supports the Cromemco scheme of bank select. It can also be programmed through the use of jumpers to "come up" in either the "on" or "off" condition.

Seattle Computer Products, Inc.
1114 Industry Drive • Seattle, WA 98188

Rev. C

Configuring the System

No changes are required to the 16K PLUS RAM board for it to interface with the majority of the systems now on the market. Listed below are the more popular systems along with specific directions for configuring the 16K PLUS board for that particular system.

Cromemco Z2D, Etc.

For operation in the lowest 48K of memory space:
1. "V" jumper should be changed to position "1".
2. Set Bank Select Switch segment "0" to "on".
3. Set addresses on RAM board using S1 and S2.

For operation in the highest 16K of memory space:
1. "V" jumper should be changed to position "1".
2. Set Bank Select Switch segment "0" to "on".
3. Set addresses on RAM board using S1 and S2.
4. Change jumper "Z" from 1 to 2.

For operation above first 64K of memory space:
1. "V" jumper should be changed to position "1".
2. Set Bank Select Switch segments to desired bank (bank 0 is off).
3. Set addresses of RAM board using S1 and S2.
4. IF using lowest 48K of any bank, THEN no other changes required.
5. IF using highest 16K in any bank, THEN:
5a. Change jumper "Z" from 1 to 2.
5b. On Cromemco Disk Controller Card — set switch 2 to "on".

North Star Horizon

1. Set addresses of RAM board using S1 and S2.
2. "V" jumper should remain in position "2".

IMSAI 8080

1. Set addresses of RAM board using S1 and S2.
2. "V" jumper should remain in position "2".

Poly 88

1. Set addresses of RAM board using S1 and S2.
2. "V" jumper should remain in position "2".

Altair 8080 A or B

1. Set addresses of RAM board using S1 and S2.
2. "V" jumper should remain in position "2".

Sol 20

1. Set addresses of RAM board using S1 and S2.
2. "V" jumper should remain in position "2".

Alpha Micro

For operation in the lowest 60K of memory space:
1. Defeat "bank Select" by removing jumper "T — T".
2. "V" jumper should be changed to position "1".

With the board configured as described above, up to 60K of 16K PLUS memory may be used in an Alpha Micro system. Typically boards will be addressed as follows:

Board 1 — 0, 1, 2, and 3.
Board 2 — 4, 5, 6, and 7.
Board 3 — 8, 9, A, and B.
Board 4 — C, D, and E.

To use the maximum of 63K of RAM, a modification of the AM-200 Disk Controller card is necessary. On the back of the Disk Controller card, connect a jumper from Z49, pin 15, to the board edge connector pin 67. (Z49 is a 74367, located just to the right of the 2708 ROM and near the edge connector.) Use care while soldering to the edge connector to make certain the solder covers only the top 1/16 inch of the edge connector pin.

Now — ONLY on RAM board 4, add a jumper between the pads labeled "Y - Y".

The address switches on board 4 should be set to C, D, E, and F.

The purpose of these changes is to use the Phantom signal (pin 67 of the S-100 bus) to disable the RAM board whenever the ROM on the AM-200 Disk Controller board is enabled.

Other Systems

In most systems, the 16K PLUS board will work properly as received from the factory with only address setting required. If it does not work immediately, try changing the "V" jumper from "1" to "2". If this does not cause the board to function properly, it will be necessary for you to read the section "Configuring Your Board".

Ram Board Addressing

The address of the RAM board is selected by throwing segments of the DIP switches 1 and 2 to the "on" position. These two switches are the top two DIP switches on the board.

Memory Slots

The number (O through F) on the left side of the two DIP switches represent the 16 possible 4K "slots" which most CPUs are capable of directly addressing.

Memory Blocks

The numbers (1 through 4) on the right side of the two DIP switches represent the four "blocks" into which the memory board has been divided. Each "block" is 4K in size.

Upon examination of the board, it will be seen that each "block" can be connected to four possible 4K slots. For example: block 1 can be connected (by throwing the DIP switch segment opposite it to the "on" position) to memory slots 0, 4, 8, and C. Block 2 can be connected to memory slots 1, 5, 9, and D, etc.

Normal Address Selection

Normally, four successive memory slots will be lected for the board. As an example: selection of the lowest 16K of address space for this board is accomplished by throwing the switch segments opposite slots 0 through 3 to the "on" position. Selecting the second 16K would be accomplished by throwing the switches opposite slots 4 through 7 to the "on" position.

If it was desirable to locate half of the RAM board in the lowest 8K and half at the highest 8K, this could be accomplished by setting the switches opposite memory slots "0" and "1" to "on" for the lowest 8K and the memory switches opposite "E" and "F" to "on" for the highest 8K.

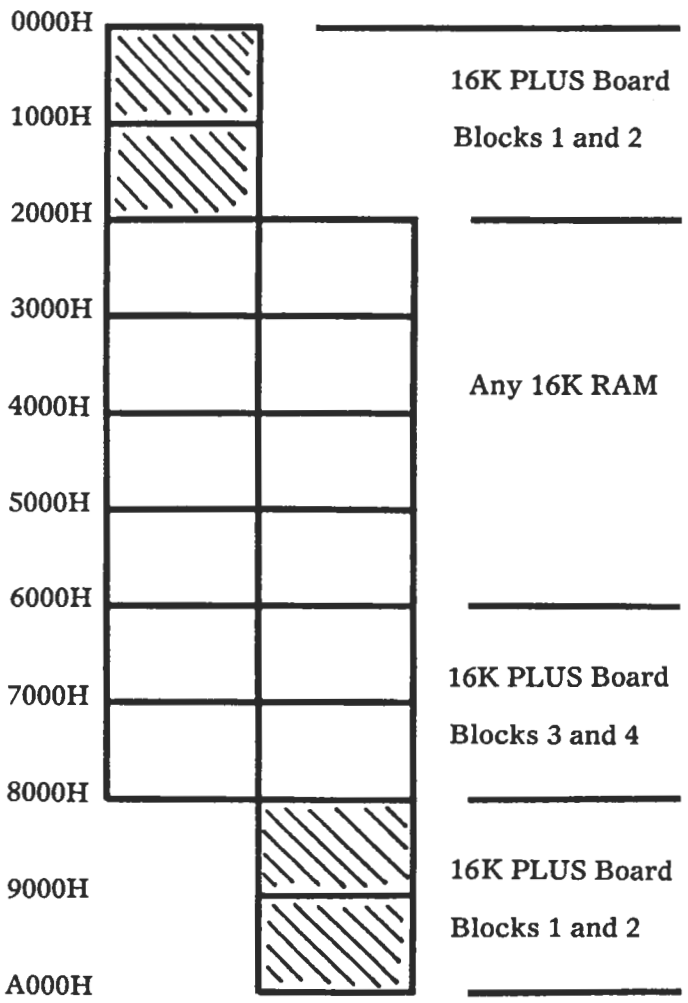
Note that in all of these "normal" address selection cases, each "block" is addresses by **one and only one** memory slot address.

Parallel Addressing

Parallel Addressing allows you to have your RAM located at one address for one type of software and at another address for another type of software. This feature helps take care of the problem you run into when your software has different starting addresses.

An example may help illustrate this problem. North Star software begins at 2000H. Perhaps your "game package" begins at 0000H. Do you "waste" e lowest 8K while running North Star Basic?

There are several solutions. One, you can buy 64K of RAM and forget the problem. Two, you can physically "relocate" RAM whenever you switch software. Or, three, you can use "parallel addressing".



Parallel Addressing

The above memory map illustrates how "parallel addressing" may be used to make 32K of RAM look like 40K to the computer. Two 4K blocks of RAM are parallel addressed at both 0000H through 1FFFH and 8000H through 9FFFH.

For software originating at 0000H, you have 32K of RAM running from 0000H to 7FFFH. For software originating at 2000H, you have 32K of RAM running from 2000H to 9FFFH. You can switch RAM origin "on the fly" without any physical change to the board. The two 4K blocks which are parallel addressed are shown cross hatched on the figure. Other parallel addressing schemes will also work.

Bank Select

"Bank Select" is the name of the system devised for increasing the amount of RAM accessible by a microprocessor to more than the 64K selectable by address bits. The system developed by Cromemco is the most widely used and is implemented on the RAM board.

The Cromemco system allows access to 512K of RAM organized in eight "banks", each containing 64K. The various "banks" are turned on or off by software commands using Output Port 40H.

Your RAM board contains a Bank Select Switch (S-3, the bottom of the three DIP switches) with segments corresponding to the eight "banks". To have the Bank Select Output Command turn the RAM board "on", the Bank Select Switch segment corresponding to the bank selected must be in the "on" position.

The following table shows the effect of various command words over the 40H Output Port.

Bit	7	6	5	4	3	2	1	0	Effect on RAM boards
	0	0	0	0	0	0	0	0	Disables all RAM boards
	0	0	0	0	0	0	0	1	Enables all boards to bank 0. Disables all in other banks.
	0	0	0	0	0	0	1	0	Enables all boards in bank 1. Disables all in other banks.
	0	0	0	0	0	1	0	0	Enables all boards in bank 2. Disables all in other banks.
	0	0	0	0	1	1	0	0	Enables all in banks 3 and 2. Disables all in other banks.

SPECIAL NOTE: A normal Cromemco "boot" sends a command to Output Port 40H to "turn on" bank 0. The same output command **"turns off"** all boards which were not bank addressed at 0. Whether your board is on or off can be determined by observing the LED. It is "on" when the board is on.

Board Configuration Jumpers

RAM Enable / Disable

Jumper "Z", located to the right of DIP switch 2, is used to select whether the board "comes up" on or off. As received from the factory, the "Z" jumper is connected to "1" which causes the board to come up in the on or enabled condition.

If your system is a Cromemco with a disk and you are using 64K of RAM, the board addressed to the highest 16K must "come up" in the disabled condition to prevent a conflict with a ROM in the system. To cause your board to do this requires that you cut the PC board trace between the pad labled "Z" and the pad labled "1". Then, jumper between pads "Z" and "2".

POC/ PRESET Option

As received from the factory, PRESET (active low) is used to trigger the enabling or disabling (depending on the "Z" jumper selection) of the board. If it is desirable to have the POC (active low) signal perform this triggering function, cut the printed circuit board trace between "X" and "1" (located in the lower right-hand corner of the board). Then, jumper between "X" and "2".

SOUT Option

Most systems use the SOUT signal. If your system is one of the few which does not, defeat the SOUT input by cutting the printed circuit board

race between pads "W -W". This is located near he center of the board just below U57.

MWRITE / PWR Option

This option allows you to select the source of the write pulse. Most systems support MWRITE and this is the option selected at the factory. If your system does not provide MWRITE or the RAM board does not function well using MWRITE, select PWR by changing jumper "V" from "2" to "1". This jumper is located in the lower right-hand corner of the RAM board.

PHANTOM

Some Processor Technology systems use bus line 67 for a Phantom (active low) signal which disables RAM while a ROM, co-located in the same address space, is being read. If your system uses this signal, jumper between pads "Y -Y". They are located near the center of the board and the edge connector.

BANK SELECT Disable Option

Bank Select may be disabled so the board is always "on". This action may be desirable if your software uses output port 40H for some function other than Bank Select. To disable Bank Select, pull the jumper wire between pads "T -T". The jumper is located in the top right-hand corner of the board.

Theory of Operation

The key to understanding the operation of the 6K PLUS RAM board circuitry is to consider it a "memory array" with supporting circuits to buffer inputs and outputs and control circuits for determining when a read of a write operation is called for.

It is suggested that you follow along on the schematic while reading this section.

Memory Array

The Memory Array includes 32 4K by 1 static RAM chips (4044 or 5257) organized into four blocks of 4K by 8 bits each. All address changes or write commands are fed to all 32 chips; however, only the block of eight chips "selected" by the low Chip Select signal will be active.

Data to the board (CPU Data Out Bus) is also continually being sent to all 32 chips, however, to "write" new data into the chips requires several actions including a low CS signal to the particular block and a write command. The output buffers on the chips are in the "high impedance state" unless the chip is selected by the low CS signal.

Note the identification of the chips: U11 is block , bit 1; U12 is block 1, bit 2; etc. In general, the first digit of the IC number in the Memory Array designates the "block" while the second number designates the bit position.

Address Buffers

Address line A-0 through A-11 are buffered by 74LS240 buffers. These buffers provide hysterisis inputs (Schmitt trigger) and low loading to the system bus. They are capable of high current output for fast switching of address information in the Memory Array. These buffers are enabled at all times so the address information at the chips continually follows the bus.

Block Select

The Block Select circuitry accepts addresses A-12 through A-15 as well as SOUT and the state of "Bank Select" as inputs. It decodes these inputs to determine if this particular RAM board is being addressed.

If the bank select is low, this board is disabled and no reads or writes are possible with it. If the SOUT signal is high, this indicates an "output port" is being addressed and the Block Select part of the board remains disabled.

Assuming bank select is high (the board is enabled) and SOUT is low, the Block Select circuitry decodes the A-11 through A-15 to obtain a unique low signal on one of the sixteen outputs of the two 74LS156 decoders. If this "low" output corresponds to a switch segment of S1 or S2 which is "closed", the Chip Select line connected to the switch is pulled low, enabling that block of RAM in the Memory Array.

Note for addressing purposes that each Chip Select line will respond to only four 4K slots out of the sixteen available. For example; Chip Select line CS1 will respond to addresses 0XXXH, 4XXXH, 8XXXH, and CXXXH only.

Normal addressing procedure is to connect each 4K RAM block to only one of the 16 possible "memory slots". If more than one is connected, the block of RAM will respond to more than one address. This is called "parallel addressing". Parallel addressing offers the system user certain advantages which were discussed earlier.

Memory Write

For a memory write to occur, two actions must take place. Depending on which write option was selected, either PWR must be low or MWRITE

must be high and the chip block must have been selected by the chip select line. Once these two conditions have been met (and minimum data setup times have also been met) whatever data that is presented to the RAM chips will be stored.

Data Out Buffers

The Data Out Buffers are contained in U6, a 74LS240. It provides high driving current to the bus. The buffers will source 3 ma. and sink 24 ma. and should operate without difficulty in all systems including those with bus terminators. The Data Out Buffers are controlled by the Data Out Buffer Control Circuit.

Data Out Buffer Control

The Data Out Buffer Control circuit consists of three sections of U7 and its inputs. If this particular board is addressed, the output on pin 8 of U53 goes high enabling the remainder of the circuit. If both SMEMR and PDBIN go high, the Data Out Buffer Enable signal (pin 6 of U7) will go low, enabling the Data Out Buffers.

Data In Buffers

The Data In Buffers are contained in U5, a 74LS240. This chip provides low loading on the bus lines and has hysterisis inputs (Schmitt trigger) for high noise immunity.

Bank Select

Bank Select is a method of extending the addressable range of memory beyond the normal 64K. It operates through software control to provide the system user with eight separate "banks" of memory, each containing 64K. This board uses the scheme made popular by Cromemco and is compatible with Cromemco software.

The banks select circuitry is located on the lower left corner of the schematic. The bank select flip-flop, U55, stores the last bank select command. This FF can be set or cleared by POC or PRESET (both active low). As delivered from the factory and as shown on the schematic, PRESET (active low) pulls down pin 10 of the FF and sets it in the bank select enabled condition. (Most systems output a PRESET (active low) command on power up.)

In the event you want your system to "come up" in the board disabled condition (such as with a Z2D with the board located in the highest 16K of address space). jumper "Z" is changed from "1" to "2". This "clears" the FF and disables bank select when PRESET (active low) is received.

Software control of bank select is accomplished through use of output port 40H and the "Data Out" lines. "Output Port 40H" is decoded by U56 and part of U53 to provide a "clock" for the FF. This clock latches the output state of U60 into the FF. The state of U60 is determined by the states of DOO through DO7 and the position of the Bank Select Dip Switch (S-3).

To turn on the board, a "one" is outputted on this port on the bit position corresponding to the DIP switch segment which is "on". Assume that switch segment "O" is on. A "one" is inverted by the Data In Buffer and presents a low signal to the DIP switch and then to pin 1 of U60. This low causes the output of U60 to go high. This "high" is latched into the FF to enable bank select.

If the output signal on the bus had been "low", a low would have been latched into the FF and bank select would go low, disabling the board. Also, if all the bank select switches were "open" when the bank select command was outputted, the board would be disabled. This last is caused because all of the inputs of U60 are held high by the pull-up resistors.

The Bank Select function will be disabled and board remain "on" if jumper "T-T" is pulled. Pulling this jumper prevents any signals from output port 40H from altering the state of the FF after it was originally set by the PRESET (active low) signal.

Power System

The Power System consists of four nearly identical circuits. Considering the one containing U1, C1 prevents oscillations of the regulator input circuit. C5, C10, C11 and C12 provide transient suppression on the +5 volt output line. Bus bars are used for this design. They provide a very low impedance power distribution line and greatly reduce voltage transients on the line. The regulator provides both overcurrent and thermal shutdown in the event of a fault on the +5 volt line.

Repair Service

Repair service is available at the factory for any products sold by Seattle Computer Products. For items under warranty, there is no charge for this service.

For repair of this board when it is no longer under warranty, return the board along with a check for $25 to the address listed below. If the repair and return of the board can be accomplished for under the $25, the balance will be refunded to you. If the cost of repair exceeds $25, you will be notified and you will have the option of us returning both the board and your check or having us go ahead with the repair.

Normal factory repair time is 48 to 72 hours. Ship all returned boards to:

Seattle Computer Products
1114 Industry Drive
Seattle, Washington 98188

Specifications

16K PLUS RAM Board

Electrical Characteristics

Parameter	**Min**	**Typ***	**Max**	**Units**
Power Supply Voltage	7.5		13.5	volts
Power Supply Current		1.8		amps
High Level Signal Input	2.0		5.5	volts
Low Level Signal Input	-0.5		0.8	volts
High Level Input Current				
All lines			20	uamps
Low Level Input Current				
A-0—A-14, DO-0—DO-7			200	uamps
All other			400	uamps
Hysteresis				
A-0—A-14, DO-0—DO-7	0.2	0.4		volts
All others	0.4	0.8		volts
Data Out Voltage				
High level—3 ma source	2.4	3.4		volts
Low level—24 ma sink		0.35	0.5	volts
High Z current	-20		+20	uamps

AC Characteristics (Worst case conditions)

Chip Speed	250 nsec.	450 nsec.
Access and read times (nsec)	286	486
Write cycle times	268	468

Thermal Characteristics

Operating Environment Temperature 5 to 65 degrees Centigrade

*Typ. is at 25 degrees Centigrade

One-Year Limited Warranty

Warrantee and Warranty Period

The Seattle Computer Products (hereinafter referred to as SCP) Warranty for this product extends to the original purchaser and all subsequent owners of the product for a period of one year from the time the product is first sold at retail and for such additional time as the product may be out of the owner's possession for the purpose of receiving warranty service at the factory.

Warranty Coverage — Factory Assembled Units Purchased by USA Customers

This product, when assembled by the SCP factory, is warranted to be free from defects in material and workmanship and to perform within the specifications detailed in the product manual during the period of the warranty. *This warranty does not cover damage and is void if the product has been damaged by neglect, accident, unreasonable use, improper repair, or other causes not arising out of defects in materials or workmanship.*

Warranty Coverage — Factory Assembled Units Purchased by Foreign Customers

Because of the large cost and time delays caused by going through customs twice for a unit shipped outside the USA and then returned for repair, *labor is not warranted for this product when it is shipped outside the United States of America.*For this case, the product is warranted to be free from defects of material only.

Warranty Coverage — Units Purchased as Kits

Since labor is not under the control of SCP for units sold as kits, the product is warranted to be free from defects of material only.

Warranty Performance

During the warranty period, SCP will repair or replace defective boards or components upon written notice that a defect exists. Defective memory ICs or certain other high value parts must be returned to SCP. Other components will be replaced without the part having to be returned to the factory *with the exception that SCP retains the right in all cases to examine the defective board prior to component replacement under the warranty.* In the event the return of the board or part is requested by SCP under this warranty, the owner shall ship the board or part prepaid to the SCP factory. SCP will pay for shipment of boards or parts to the owner. All repairs or replacements by SCP under this warranty will be performed within five working days following receipt of notice of defect or return of components as called for under this warranty.

Warranty Disclaimers

While high reliability was a major design factor for this product and care is used in its manufacture, no certainty can be achieved that any particular product will operated correctly for any specific time. No representation is made by SCP that this product will not fail in normal use. Because of inability to guarantee 100% reliability, *SCP shall not be liable for any consequencial damage the user may suffer because the product fails to function reliably 100% of the time.* Any implied warranties arising from the sale of this product are limited in duration to the warranty period defined above.

Legal Remedies

The warranty gives the purchaser specific legal rights. He may have additional rights which vary from state to state.

Shipping Instructions

In the event it becomes necessary to return the product or components to SCP, also return a written explanation of the difficulty encountered along with your name, address and phone number. Package the items in a crushproof shipping container with adequate packing material to prevent damage and ship prepaid to:

Seattle Computer Products
1114 Industry Drive
Seattle, Washington 98188

Seattle Computer Products, Inc.
1114 Industry Drive • Seattle, WA 98188 • (206) 255-0750

ERRATA SHEET

16K PLUS RAM - Revision C

Page 3 - Configuring the System

Under "Cromemco Z2D, Etc.

For Operation in the highest 16K of memory space:"

After 4, add

5. On Cromemco Disk Controller Card--set switch 2 to "on".

Page 3 - Configuring the System

Under "North Star Horizon"

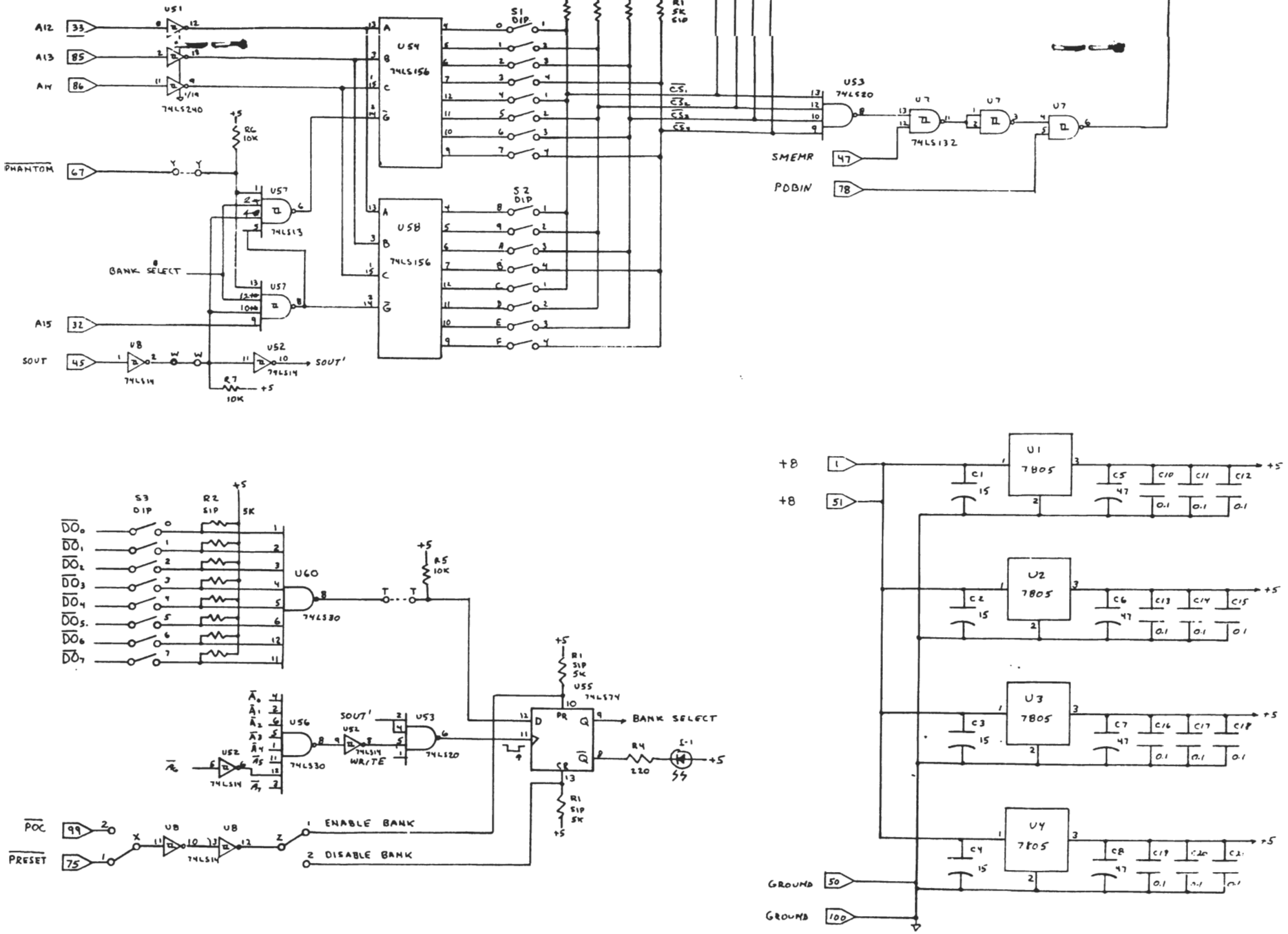
After 2, add

3. It may be necessary to change the "X" jumper.
(See POC/PRESET option description on page 5)

Page 3 - Configuring the System

Under "Other Systems"

As shipped from the factory, the "V" jumper is in position "2". This paragraph should indicate it may be necessary to change this jumper to position "1".



16K PLUS

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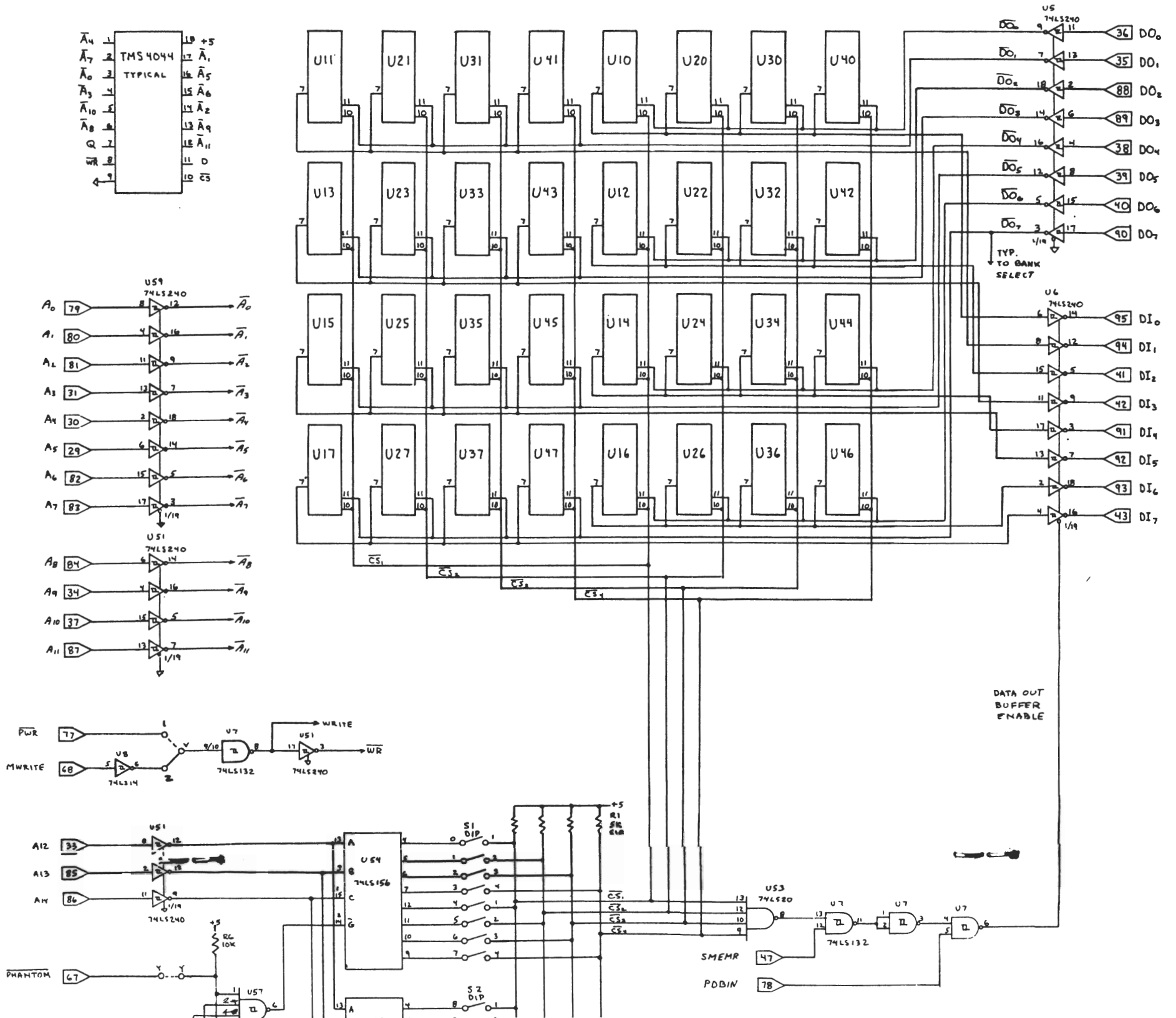
TMS 4044
TYPICAL
U11
U21
U31
U41
U10
U20
U30
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U27
U37
U47
U16
U26
U36
U46
U5
74LS240
U6
74LS240
U59
74LS240
U51
74LS240
TYP.
TO BANK
SELECT
DATA OUT
BUFFER
ENABLE
WRITE
MWRITE
PWR
74LS32
74LS14
U54
74LS156
S1
DIP
S2
DIP
U53
74LS20
74LS132
SMEMR
PDBIN
PHANTOM
U57